



# UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE  
United States Patent and Trademark Office  
Address: COMMISSIONER FOR PATENTS  
P.O. Box 1450  
Alexandria, Virginia 22313-1450  
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
-----------------	-------------	----------------------	---------------------	------------------

10/751,129

12/31/2003

Anees Narsinh

134171

1739

35114 7590 02/04/2008

ALCATEL LUCENT  
(FKA ALCATEL INTERNETWORKING, INC.)  
INTELLECTUAL PROPERTY & STANDARDS  
3400 W. PLANO PARKWAY, MS LEGL2  
PLANO, TX 75075

EXAMINER

SHIN, KYUNG H

ART UNIT

PAPER NUMBER

2143

MAIL DATE

DELIVERY MODE

02/04/2008

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

<b>Office Action Summary</b>	Application No. 10/751,129	Applicant(s) NARSINH ET AL.	
	Examiner Kyung H. Shin	Art Unit 2143	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

### Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

### Status

- 1) ☒ Responsive to communication(s) filed on 15 November 2007.
- 2a) ☒ This action is **FINAL**.                      2b) ☐ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

### Disposition of Claims

- 4) ☒ Claim(s) 1-14 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.
- 5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.
- 6) ☒ Claim(s) 1-14 is/are rejected.
- 7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.
- 8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

### Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

### Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All    b) ☐ Some \*    c) ☐ None of:
1. ☐ Certified copies of the priority documents have been received.
  2. ☐ Certified copies of the priority documents have been received in Application No. \_\_\_\_\_.
  3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

### Attachment(s)

- |  |   |
|--|---|
| 1) <input checked="" type="checkbox"/> Notice of References Cited (PTO-892)                                | 4) <input type="checkbox"/> Interview Summary (PTO-413)<br>Paper No(s)/Mail Date. _____ |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948)                       | 5) <input type="checkbox"/> Notice of Informal Patent Application                       |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO/SB/08)<br>Paper No(s)/Mail Date _____ | 6) <input type="checkbox"/> Other: _____  |

### DETAILED ACTION

1. Application was filed on **12-31-2003**.
2. Claims **1 - 14** are pending. Claims **1, 2** have been amended. Claims **1, 2** are independent.

### *Response to Arguments*

3. Applicant's arguments filed 11/15/2007 have been fully considered but they are moot due to new grounds of rejection.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims **1 - 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Crinion et al.** (US Patent No. **6,181,699**) in view of **Denney et al.** (US PG PUB No. **20030061623**).

**Regarding Claim 1**, Crinion discloses a data link layer processor comprising:

- a) one or more media access controllers (MACs) for receiving a frame from a communication network; (Crinion Figure 8 (210a, 210b); col. 5, ll 66-67; col. 6, l 66 - col. 7, l 6: multiple ports, MACs; incoming data, reception of data frame)

- c) a statistics acquisition module, operatively coupled to the one or more MACs, for compiling statistics associated with each of the plurality of MACs. (Crinion col. 5, ll 53-56; col. 6, ll 50-54; col. 7, ll 53-56: after frame sent, signal to transmit statistics, network management statistics, MIB counters)

Crinion does not specifically disclose that each MAC includes a MAC preprocessor and a MAC postprocessor. However, **Denney** discloses:

- b) each of the one or more MACs includes a MAC preprocessor and a MAC postprocessor, (Denney para 052, ll 1-4: MAC preprocessor, postprocessor)

It would have been obvious to one of ordinary skill in the art to modify Crinion as taught by Denney where each MAC includes a MAC preprocessor and a MAC postprocessor. One of ordinary skill in the art would have been motivated to employ the teachings of Denney in order to increase packet throughput capacity and sustain performance. (Denney para 017, ll 1-3: “ ... *Therefore, a system and method that increase packet throughput capacity and sustain performance are needed to address the above problems. ...* ”)

**Regarding Claim 2**, Crinion discloses a switching device comprising:

- a) one or more physical layer interfaces for receiving one or more frames from a communication network; (Crinion Figure 8 (210a, 210b); col. 5, ll 66-67; col. 6, ll 66 - col. 7, ll 6: multiple ports (MACs), reception of data frames; col. 5, ll 26-29: Ethernet (network) communications of frame data)
- b) a plurality of data link layer processors (Crinion Figure 8 (210a, 210b); col. 5, ll

26-28; col. 8, ll 17-19: data link layer (MAC) processor(s), 802.3 LAN users), wherein each data link layer processor comprises:

- c) one or more media access controllers (MACs), wherein each MAC is operatively coupled to a physical layer interface; (Crinion Figure 8 (210a, 210b): multiple ports (MACs); col. 5, ll 66-67; col. 6, l 66 - col. 7, l 3: interface to PHYS, physical layer; col. 5, ll 26-29: MAC (Ethernet, 802.3, network communications) transmission/reception of frame data) and
- d) a statistics acquisition module, operatively coupled to the one or more MACs, for compiling statistics on each of the plurality of MACs; (Crinion col. 5, ll 53-56; col. 6, ll 52-54; col. 7, ll 53-56: network management statistics, transmit statistics to MIB engine)
- e) a network processor, operatively coupled to the plurality of data link layer processors, for routing the one or more frames received from the plurality of data link layer processors. (Crinion Figure 8; col. 2, ll 46-54: circuit data switch, send and receive data frames; col. 1, ll 7-10; col. 5, ll 17-19: routing data frames)

Crinion does not specifically disclose that each MAC includes a MAC preprocessor and a MAC postprocessor. However, Denney discloses each of the one or more MACs includes a MAC preprocessor and a MAC postprocessor. (Denney para 052, ll 1-4: MAC preprocessor, postprocessor)

It would have been obvious to one of ordinary skill in the art to modify Crinion as taught by Denney where each MAC includes a MAC preprocessor and a MAC

postprocessor. One of ordinary skill in the art would have been motivated to employ the teachings of Denney in order to increase packet throughput capacity and sustain performance. (Denney para 017, II 1-3)

**Regarding Claim 3**, Crinion discloses the switching device of claim 2, wherein each of the data link layer processors further comprises one or more flow search engines for classifying the one or more frames based upon one or more properties associated with the frames. (col. 1, II 47-49; col. 3, II 26-27: assign or change priority level (property) of data frames, and priority circuit writes priority (property) information)

**Regarding Claim 4**, Crinion discloses the switching device of claim 3, wherein one or more properties comprise a source port, a VLAN tag state, a VLAN identifier, and a VLAN tag control information (TCI) field. (col. 1, II 50-52; col. 2, II 1-3: assign VLAN tag; col. 3, II 62-64: VLAN tag, Tag Control Information (TCI))

**Regarding Claim 5**, Crinion discloses the switching device of claim 3, wherein the one or more flow search engines comprise one or more content addressable memories (CAMs). (col. 1, II 52-54: search circuit; col. 2, II 46-51; col. 2, II 55-57: circuit: content addressable memory (CAM) and search circuit)

**Regarding Claim 6**, Crinion discloses the switching device of claim 5, wherein the one or more CAMs associated with each of the plurality of data link layer processors

consists of QoS rules pertaining to the associated plurality of physical layer interfaces.  
(col. 2, ll 57-59; col. 3, ll 19-23: content addressable memory stores priority information  
(QoS); col. 1, ll 47-49; col. 3, ll 26-27: set priority, determination of quality of service  
(QoS) for data frame(s))

**Regarding Claim 7**, Crinion discloses the switching device of claim 2, wherein data link  
layer processors are media access controller (MAC) processors. (Figure 8 (210a, 210b):  
ports, MAC (data link layer, layer 2 OSI protocol); col. 5, ll 66-67; col. 6, l 66 - col. 7, l 3:  
MAC layer (data link layer) frames information)

**Regarding Claim 8**, Crinion discloses the switching device of claim 2, wherein the  
switching device is selected from the group consisting of: a router, a multi-layer  
switching device, and a switch blade. (col. 2, ll 46-53; col. 4, ll 45-48: circuit, switch  
(switching device))

**Regarding Claim 9**, Crinion discloses the switching device of claim 2, wherein the  
statistics compiled by the statistics acquisition module comprise ingress frame statistics.  
(col. 5, ll 53-56; col. 6, ll 52-54; col. 7, ll 53-56: network management statistics; transmit  
statistics to MIB engine, incoming (ingress) packets)

**Regarding Claim 10**, Crinion discloses the switching device of claim 9, wherein the  
ingress frame statistics are compiled as a function of VLAN entry. (Crinion col. 9, l 66 -

col. 10, l 2: data frame received as VLAN tag processing, packets filtered based on VLAN information; col. 5, ll 53-56; col. 6, ll 52-54; col. 7, ll 53-56: statistics for incoming packets (data frames), maintain set of MIB counters statistics)

**Regarding Claim 11**, Crinion discloses the switching device of claim 10, wherein the ingress frame statistics compiled as a function of VLAN entry comprise: the number of bytes enqueued at the data link layer processor; the number of frames enqueued at the data link layer processor; the number of non-unicast bytes enqueued at the data link layer processor; and the number of non-unicast frames enqueued at the data link layer processor. (Crinion col. 5, ll 53-56; col. 6, ll 50-54; col. 6, l 9-11; col. 7, ll 53-56: MIB counter statistics, counters (unicast packets, incoming packets, frames sent)

**Regarding Claim 12**, Crinion discloses the switching device of claim 2, wherein the statistics compiled by the statistics acquisition module comprise egress frame statistics. (Crinion figure (210a, 210b); col. 5, ll 53-56; col. 6, ll 50-54: MIB counters for data frames, data frames sent (egress, output))

**Regarding Claim 13**, Crinion discloses the switching device of claim 12, wherein egress frame statistics are compiled as a function of physical layer interface. (Figure 8 (210a, 210b); col. 5, ll 53-56; col. 6, ll 48-54: MIB counters for data frames, data frames sent (egress, output), transmit data using physical layer interface)



**Regarding Claim 14**, Crinion discloses the switching device of claim 13, wherein egress frame statistics are further compiled as a function of VLAN entry. (col. 9, l 66 - col. 10, l 2: data frame received as VLAN tag processing, packets filtered based on VLAN information; col. 5, ll 53-56; col. 6, ll 50-54: statistics for sent packets (data frames), maintain set of MIB counters statistics)

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyung H. Shin whose telephone number is (571) 272-

Application/Control Number:  
10/751,129  
Art Unit: 2143

Page 9

3920. The examiner can normally be reached on 9:30 am - 6 pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

Kyung Hye Shin  
Patent Examiner  
Art Unit 2143

KHS  
January 29, 2008

/Bunjoo Jaroenchonwanit/  
Bunjoo Jaroenchonwanit  
Supervisory Patent Examiner  
Art Unit 2152  
February 1, 2008

### DETAILED ACTION

1. Application was filed on **12-31-2003**.
2. Claims **1 - 14** are pending. Claims **1, 2** have been amended. Claims **1, 2** are independent.

### *Response to Arguments*

3. Applicant's arguments filed 11/15/2007 have been fully considered but they are moot due to new grounds of rejection.

### *Claim Rejections - 35 USC § 103*

4. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which the subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

5. Claims **1 - 14** are rejected under 35 U.S.C. 103(a) as being unpatentable over **Crinion et al.** (US Patent No. **6,181,699**) in view of **Denney et al.** (US PG PUB No. **20030061623**).

**Regarding Claim 1**, Crinion discloses a data link layer processor comprising:

- a) one or more media access controllers (MACs) for receiving a frame from a communication network; (Crinion Figure 8 (210a, 210b); col. 5, ll 66-67; col. 6, l 66 - col. 7, l 6: multiple ports, MACs; incoming data, reception of data frame)
- c) a statistics acquisition module, operatively coupled to the one or more MACs, for

compiling statistics associated with each of the plurality of MACs. (Crinion col. 5, ll 53-56; col. 6, ll 50-54; col. 7, ll 53-56: after frame sent, signal to transmit statistics, network management statistics, MIB counters)

Crinion does not specifically disclose that each MAC includes a MAC preprocessor and a MAC postprocessor. However, **Denney** discloses:

- b) each of the one or more MACs includes a MAC preprocessor and a MAC postprocessor, (Denney para 052, ll 1-4: MAC preprocessor, postprocessor)

It would have been obvious to one of ordinary skill in the art to modify Crinion as taught by Denney where each MAC includes a MAC preprocessor and a MAC postprocessor. One of ordinary skill in the art would have been motivated to employ the teachings of Denney in order to increase packet throughput capacity and sustain performance. (Denney para 017, ll 1-3: “ ... *Therefore, a system and method that increase packet throughput capacity and sustain performance are needed to address the above problems. ...* ”)

**Regarding Claim 2**, Crinion discloses a switching device comprising:

- a) one or more physical layer interfaces for receiving one or more frames from a communication network; (Crinion Figure 8 (210a, 210b); col. 5, ll 66-67; col. 6, ll 66 - col. 7, l 6: multiple ports (MACs), reception of data frames; col. 5, ll 26-29: Ethernet (network) communications of frame data)
- b) a plurality of data link layer processors (Crinion Figure 8 (210a, 210b); col. 5, ll 26-28; col. 8, ll 17-19: data link layer (MAC) processor(s), 802.3 LAN users),

wherein each data link layer processor comprises:

- c) one or more media access controllers (MACs), wherein each MAC is operatively coupled to a physical layer interface; (Crinion Figure 8 (210a, 210b): multiple ports (MACs); col. 5, ll 66-67; col. 6, l 66 - col. 7, l 3: interface to PHYS, physical layer; col. 5, ll 26-29: MAC (Ethernet, 802.3, network communications) transmission/reception of frame data) and
- d) a statistics acquisition module, operatively coupled to the one or more MACs, for compiling statistics on each of the plurality of MACs; (Crinion col. 5, ll 53-56; col. 6, ll 52-54; col. 7, ll 53-56; network management statistics, transmit statistics to MIB engine)
- e) a network processor, operatively coupled to the plurality of data link layer processors, for routing the one or more frames received from the plurality of data link layer processors. (Crinion Figure 8; col. 2, ll 46-54: circuit data switch, send and receive data frames; col. 1, ll 7-10; col. 5, ll 17-19: routing data frames)

Crinion does not specifically disclose that each MAC includes a MAC preprocessor and a MAC postprocessor. However, Denney discloses each of the one or more MACs includes a MAC preprocessor and a MAC postprocessor. (Denney para 052, ll 1-4: MAC preprocessor, postprocessor)

It would have been obvious to one of ordinary skill in the art to modify Crinion as taught by Denney where each MAC includes a MAC preprocessor and a MAC postprocessor. One of ordinary skill in the art would have been motivated to employ

the teachings of Denney in order to increase packet throughput capacity and sustain performance. (Denney para 017, ll 1-3)

**Regarding Claim 3**, Crinion discloses the switching device of claim 2, wherein each of the data link layer processors further comprises one or more flow search engines for classifying the one or more frames based upon one or more properties associated with the frames. (col. 1, ll 47-49; col. 3, ll 26-27: assign or change priority level (property) of data frames, and priority circuit writes priority (property) information)

**Regarding Claim 4**, Crinion discloses the switching device of claim 3, wherein one or more properties comprise a source port, a VLAN tag state, a VLAN identifier, and a VLAN tag control information (TCI) field. (col. 1, ll 50-52; col. 2, ll 1-3: assign VLAN tag; col. 3, ll 62-64: VLAN tag, Tag Control Information (TCI))

**Regarding Claim 5**, Crinion discloses the switching device of claim 3, wherein the one or more flow search engines comprise one or more content addressable memories (CAMs). (col. 1, ll 52-54: search circuit; col. 2, ll 46-51; col. 2, ll 55-57: circuit: content addressable memory (CAM) and search circuit)

**Regarding Claim 6**, Crinion discloses the switching device of claim 5, wherein the one or more CAMs associated with each of the plurality of data link layer processors consists of QoS rules pertaining to the associated plurality of physical layer interfaces.

(col. 2, ll 57-59; col. 3, ll 19-23: content addressable memory stores priority information (QoS); col. 1, ll 47-49; col. 3, ll 26-27: set priority, determination of quality of service (QoS) for data frame(s))

**Regarding Claim 7**, Crinion discloses the switching device of claim 2, wherein data link layer processors are media access controller (MAC) processors. (Figure 8 (210a, 210b): ports, MAC (data link layer, layer 2 OSI protocol); col. 5, ll 66-67; col. 6, l 66 - col. 7, l 3: MAC layer (data link layer) frames information)

**Regarding Claim 8**, Crinion discloses the switching device of claim 2, wherein the switching device is selected from the group consisting of: a router, a multi-layer switching device, and a switch blade. (col. 2, ll 46-53; col. 4, ll 45-48: circuit, switch (switching device))

**Regarding Claim 9**, Crinion discloses the switching device of claim 2, wherein the statistics compiled by the statistics acquisition module comprise ingress frame statistics. (col. 5, ll 53-56; col. 6, ll 52-54; col. 7, ll 53-56: network management statistics; transmit statistics to MIB engine, incoming (ingress) packets)

**Regarding Claim 10**, Crinion discloses the switching device of claim 9, wherein the ingress frame statistics are compiled as a function of VLAN entry. (Crinion col. 9, l 66 - col. 10, l 2: data frame received as VLAN tag processing, packets filtered based on

VLAN information; col. 5, ll 53-56; col. 6, ll 52-54; col. 7, ll 53-56: statistics for incoming packets (data frames), maintain set of MIB counters statistics)

**Regarding Claim 11**, Crinion discloses the switching device of claim 10, wherein the ingress frame statistics compiled as a function of VLAN entry comprise: the number of bytes enqueued at the data link layer processor; the number of frames enqueued at the data link layer processor; the number of non-unicast bytes enqueued at the data link layer processor; and the number of non-unicast frames enqueued at the data link layer processor. (Crinion col. 5, ll 53-56; col. 6, ll 50-54; col. 6, l 9-11; col. 7, ll 53-56: MIB counter statistics, counters (unicast packets, incoming packets, frames sent)

**Regarding Claim 12**, Crinion discloses the switching device of claim 2, wherein the statistics compiled by the statistics acquisition module comprise egress frame statistics. (Crinion figure (210a, 210b); col. 5, ll 53-56; col. 6, ll 50-54: MIB counters for data frames, data frames sent (egress, output))

**Regarding Claim 13**, Crinion discloses the switching device of claim 12, wherein egress frame statistics are compiled as a function of physical layer interface. (Figure 8 (210a, 210b); col. 5, ll 53-56; col. 6, ll 48-54: MIB counters for data frames, data frames sent (egress, output), transmit data using physical layer interface)

**Regarding Claim 14**, Crinion discloses the switching device of claim 13, wherein



egress frame statistics are further compiled as a function of VLAN entry. (col. 9, l 66 - col. 10, l 2: data frame received as VLAN tag processing, packets filtered based on VLAN information; col. 5, ll 53-56; col. 6, ll 50-54: statistics for sent packets (data frames), maintain set of MIB counters statistics)

### ***Conclusion***

Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire **THREE MONTHS** from the mailing date of this action. In the event a first reply is filed within **TWO MONTHS** of the mailing date of this final action and the advisory action is not mailed until after the end of the **THREE-MONTH** shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than **SIX MONTHS** from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Kyung H. Shin whose telephone number is (571) 272-3920. The examiner can normally be reached on 9:30 am - 6 pm.

Application/Control Number:  
10/751,129  
Art Unit: 2143

Page 9

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David A. Wiley can be reached on (571) 272-3923. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

K H S  
Kyung Hye Shin  
Patent Examiner  
Art Unit 2143

KHS  
January 29, 2008

/Bunjob Jaroenchonwanit/  
Bunjob Jaroenchonwanit  
Supervisory Patent Examiner  
Art Unit 2152  
February 1, 2008